Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) A data processing method, comprising: [[in accordance with claim 1, further comprising:]]

receiving a plurality of combined clock-data streams according to a first clock domain, each combined clock-data stream including both clock and data signals;

dividing the plurality of combined clock-data streams into a plurality of independent clock streams and a plurality of independent data streams;

multiplexing the plurality of independent data streams and synchronizing the plurality of independent data streams to a second clock domain for processing by a framer array, the second clock domain being different from the first clock domain, the framer array being provided offset a data path of at least one of the plurality of independent data streams; and

preserving a timing of at least one of the independent clock streams according to the first clock domain during processing of the plurality of independent data streams by the framer array.

~~dividing a plurality of the one or more combined clock-data streams into a plurality of independent clock streams and a plurality of independent data streams; and~~

~~multiplexing the plurality of independent data streams for processing by the framer array, the framer array being provided offset a data path of at least one of the plurality of independent data streams.~~

3. (Previously Presented) A method in accordance with claim 2, further comprising aligning octets of at least one of the plurality of independent data streams onto a multiplexed bus,

the multiplexed bus being synchronized to the second clock domain.

4. (Previously Presented) A method in accordance with claim 3, further comprising:

demultiplexing the plurality of independent data streams;

recombining at least one independent data stream and one independent clock stream to form a recombined clock-data stream; and

re-synchronizing the recombined clock-data stream to the first clock domain.

5. (Previously Presented) A method according to claim 3, further comprising inserting status and control information to the independent data stream while the independent data stream is on the multiplexed bus.

6. (Previously Presented) A data processing system, comprising:

means for receiving a plurality of combined clock-data streams according to a first clock domain, each combined clock-data stream including both clock and data signals;

means for dividing the plurality of combined clock-data streams into a plurality of independent clock streams and a plurality of independent data streams;

means for processing the plurality of independent data streams in a second clock domain, the second clock domain being different from the first clock domain, wherein a timing of each of the plurality of independent clock streams is preserved according to the first clock domain during the processing of the plurality of independent data streams;

means for recombining corresponding ones of the plurality of independent clock data streams and the plurality of independent data streams to form a plurality of recombined clock-data streams; and

means for re-synchronizing the plurality of recombined clock-data streams to the first clock domain.

7. (Previously Presented) A data processing system according to claim 6, wherein the processing means includes means for multiplexing the plurality of independent data streams onto a common bus.

8. (Previously Presented) A data processing system according to claim 7, wherein the processing means further includes a framer state machine offset from the common bus, the framer state machine adapted to align octets of each of the plurality of independent data streams onto the common bus.

9. (Previously Presented) A data processing system according to claim 8, wherein the framer state machine is further adapted to store a context of a previous data stream processed and load a context of a current data stream.

10. (Previously Presented) A system, comprising:

a plurality of combined clock-data streams having a timing according to a first clock domain, each combined clock-data stream including both clock and data signals;

a plurality of clock paths adapted to extract clocks from the plurality of combined clock-data streams;

a plurality of data paths adapted to receive data portions of the plurality of combined clock-data streams and provide the data portions onto a common bus in a second clock domain, the second clock domain being different from the first clock domain; and

a framer state machine offset from the common bus and adapted to load and store a context for the data portions in the second clock domain,

wherein the plurality of clock paths preserve the clocks according to the first clock domain during a time that context is loaded and stored for the data portions.

11. (Previously Presented) A system according to claim 10, wherein the framer ~~unit~~ state machine is further adapted to identify a start of frames of the data portions.

12. (Previously Presented) A system according to claim 11, further comprising a plurality of synchronizers adapted to synchronize each of the plurality of data paths to the common bus according to the second clock domain.

13. (Previously Presented) A system according to claim 12, further comprising a plurality of serial-to-parallel converters coupled to the plurality of synchronizers and adapted to convert the data portions from serial data into parallel data.

14. (Previously Presented) A system according to claim 13, wherein outputs of the serial-to-parallel converters are provided to a multiplexer.

15. (Previously Presented) A system according to claim 14, wherein outputs of the multiplexer are provided to the common bus and the framer state machine.